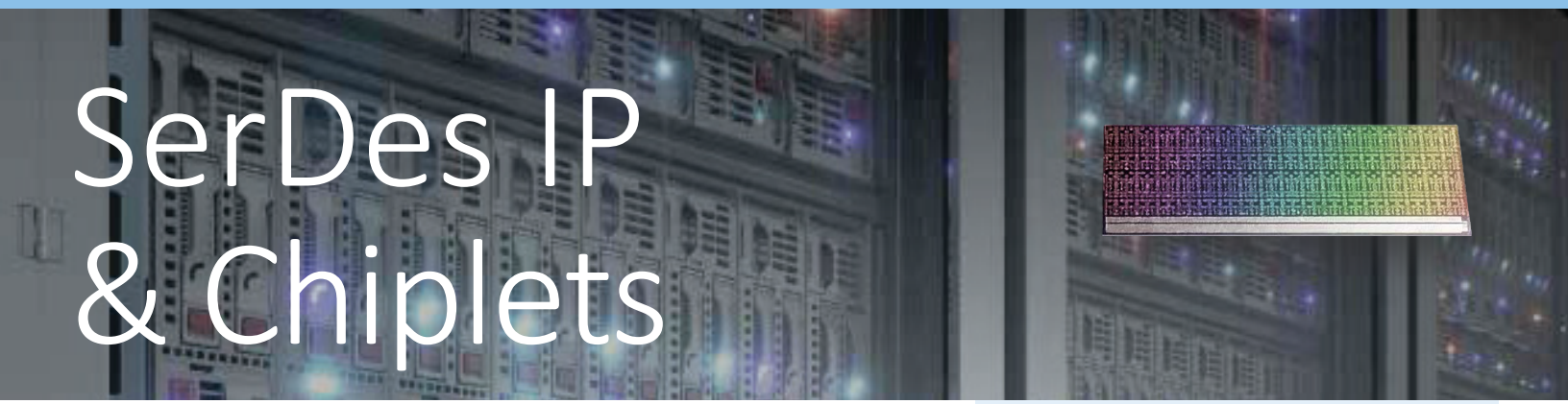


SerDes IP & Chiplets

Application Specific SerDes IP and Chip Solutions

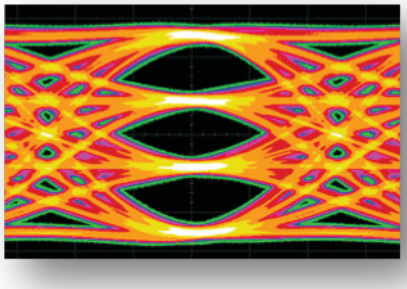
SerDes Intellectual Property (IP)

Credo designs SerDes IP that optimally balances performance, power and manufacturing process costs and risks. Our unique, patented mixed signal architecture is the foundation for our high performance and low power SerDes technology. The architectural approach taken by Credo has enabled us to design in mature fabrication processes yet deliver leading-edge performance and power. Credo was the first to deliver 56G NRZ in 40nm, 56G PAM4 in 28nm and 112G PAM4 in 28nm.

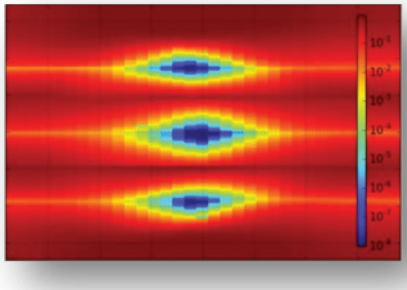
By contrast, other industry solutions have moved to power-hungry designs in the most advanced silicon processing geometries for performance, yet struggle to meet the fundamental power requirements.

PAM4 Eye Diagrams

TX



RX



SerDes IP

Credo's SerDes Intellectual Property (IP) is designed for the easy SOC integration of tens to hundreds of SerDes lanes.

- 10dB to 35dB bump-to-bump insertion loss
- Multi-rate support for 56Gbps to 112Gbps PAM4 and NRZ
- Integrated PLL
- Robust clock distribution architecture
- Advanced mixed signal analog equalization architecture
- Fully adaptive and programmable RX equalization
- Auto-negotiation
- Link Training
- Excellent random jitter performance
- Robust clock data recovery
- Complete diagnostic suite
  - On-chip PRBS generation and checking
  - RX eye monitor
  - Loop back testing
  - JTAG/IEEE 1500
- MCU per lane

Credo SerDes IP Availability

Our IP is designed for a variety of TSMC fabrication processes.

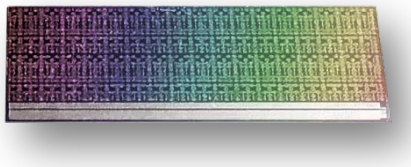
	TSMC 28nm	TSMC 16nm/12nm	TSMC 7nm
28G NRZ	MR, LR	MR, LR	MR, LR
56G PAM4		VSR, MR, LR	VSR, MR, LR
112G PAM4		XSR, VSR, MR, LR	XSR, VSR, MR, LR

Credo SerDes Chiplets

Core and analog logic may not always deploy at the same time in the same process. Maturing high performance analog typically takes longer in moving to next generation of advanced process geometries. This lagging function may slow the pace of your next generation solutions.

Credo's unique SerDes architecture has made it possible to deliver SerDes cost & power effective solutions in mature process nodes and make them available in chip form for integration with SoCs, overcoming the need for matching core logic and SerDes IP in the same process node.

Now you can fabricate your core logic in advanced processes and combine them in your SoC with Credo SerDes Chiplets, designed for high performance and low power from mature processes. You get the performance needed without delaying your time to market.



56G SerDes Chiplet

- 28nm TSMC process
- 2.5D Silicon Interposer
- Ideal for 12.8Tbps Switch Fabric ASIC

112G SerDes Chiplet

- 16nm TSMC process
- MCM/XSR and 2.5D Silicon Interposer
- Ideal for 25.6Tbps Switch Fabric ASIC

For more information please visit **www.credosemi.com** or email **sales@credosemi.**com.