

## 400G (8x56G) QSFP-DD PAM4 to 400G (8x56G) QSFP-DD PAM4

Plug & Play Active Electrical Cable for In-Rack Ethernet Applications in Distributed, Disaggregated Chassis (DDC)

### Description

Credo's HiWire™ Low Power CLOS Active Electrical Cable (LP CLOS AEC) is a thin, low power 400G AEC specifically designed for in-rack applications replacing backplanes in Distributed, Disaggregated Chassis (DDC) implementations. Plug & Play LP CLOS AECs consume up to 75% less power and take 75% less volume than DACs, enabling interconnect densities of up to 500 cables per rack.

Credo's CAC4XX321D1D-XX-HW HiWire LP CLOS AEC is designed for telecom and data center use. It can sustain 8 lanes of 56G-PAM4 signal in each direction, providing bi-directional 400Gbps traffic per cable. The use and replacement of this AEC is simple and straightforward as it adopts standard QSFP-DD type 2 form factor and complies to MSA specifications.

### Product Features

The following are the key features of the HiWire LP CLOS AEC:

- Recognizable, purple PVC jacket
- 400G to 400G data rate
- Built-in diagnostic features
- CMIS compliant
- Single 3.3V power supply
- Typ. 4.5W power dissipation each end
- BER < 10<sup>-15</sup> (post FEC)
- Hot pluggable
- RoHS2 compliant
- I<sup>2</sup>C management interface
- Operating case temperature range: 0° to +70°C



1:1 Direct LP CLOS AEC

### Product Selections

Part Number	Length	AWG	Weight
CAC4XX321D1D-C0-HW	0.5 - 2.5m*	32	CMIS 3.0
CAC4xx321D1D-D0-HW	0.5 - 2.5m*	32	CMIS 4.0
CAC4xx321D1D-A0-HW	1.75 - 2.5m*	32	788g

\*Length available in 0.25m increments

### Mechanicals

Parameter	Cable Type	Typical	Length
Diameter	16P 32AWG	6.8mm	0.5 - 3.0m

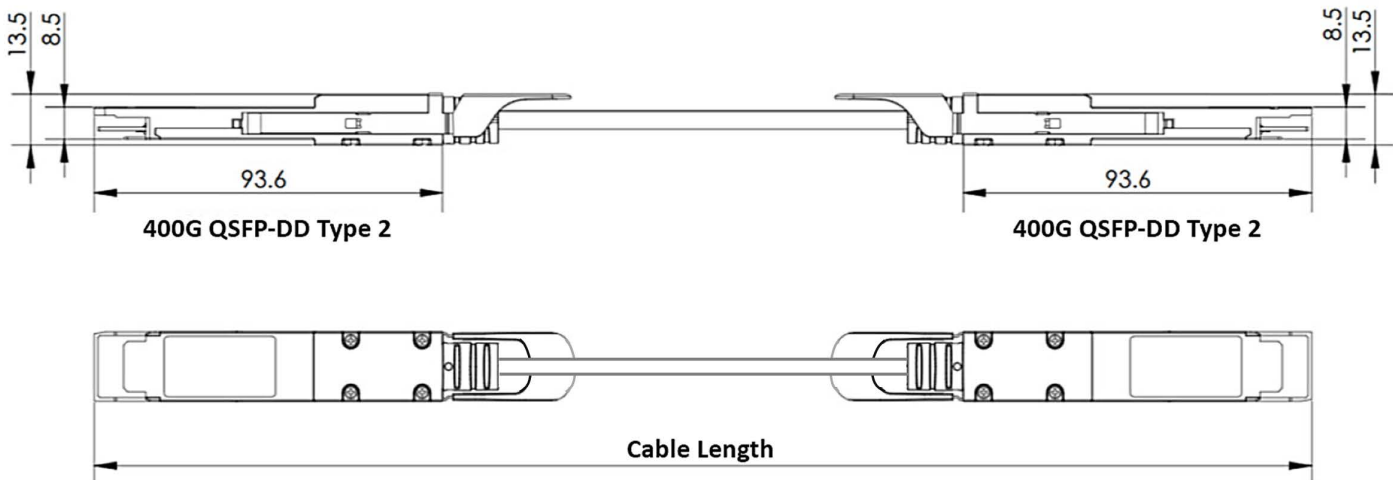
### Supported Standards

The following are the key features of the HiWire cable:

- Common Management Interface Specification (CMIS) v3.0 and v4.0
- QSFP-DD MSA v3.0

## General Product Characteristics

Parameter	Value
Module Form Factor	QSFP-DD type 2
Number of Data Lanes	8 TX and 8 RX per module (PAM4)
Maximum Aggregate Data Rate	400Gbps
Nominal Data Rate per Lane	53.125Gbps (PAM4)
Electrical Interface and Pin-out	76-pin edge connector
Pin Description	Per QSFP-DD Hardware Specification
Management Interface	I <sup>2</sup> C, serial, timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers (QSFP-DD)
Length of Copper AEC	0.5m - 2.5m in 0.25m increments
BER (Pre-FEC)*	Typ. <math>10^{-8}</math> * Tested with QPRBS31 pattern
BER (Post-FEC)*	<math>10^{-15}</math> * Tested with QPRBS31 pattern



For more information please visit [www.credosemi.com/hiwire-aec](http://www.credosemi.com/hiwire-aec) or email [hiwire@credosemi.com](mailto:hiwire@credosemi.com)

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