PRODUCT BRIEF > SERDES IP

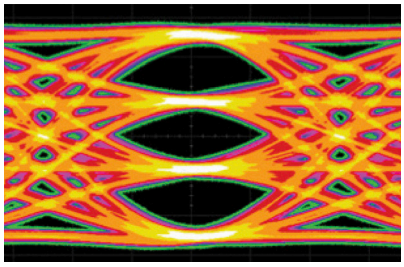
APPLICATION SPECIFIC SerDes IP and Chiplet Solutions

SerDes Intellectual Property (IP)

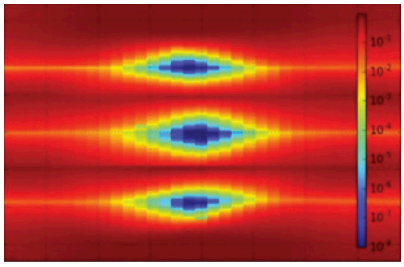
Credo designs SerDes IP that optimally balances performance, power and manufacturing process costs and risks. Our unique, patented mixed signal and DSP architectures are the foundation for our high-performance and low-power SerDes technology. The architectural approach taken by Credo has enabled us to design in mature fabrication processes yet deliver leading-edge performance and power.

Credo was the first to deliver 56G NRZ in 40nm, 56G PAM4 in 28nm, 40G PAM3 in 12nm, and 112G PAM4 in 28nm. By contrast, other industry solutions have moved to the most advanced silicon processing geometries for equivalent performance and to lower power

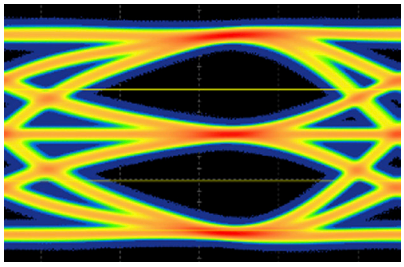
PAM4 Eye TX



PAM4 Eye RX



PAM3 Eye TX



SerDes IP

Credo's SerDes Intellectual Property (IP) is designed for the easy SOC integration of tens to hundreds of SerDes lanes.

- 10dB to 35dB bump-to-bump insertion loss
- Multi-rate support for 112G to 56G PAM4, 40G PAM3, 25G and subrate NRZ
- Integrated PLL
- Robust clock distribution architecture
- Advanced mixed signal analog equalization architecture
- Fully adaptive and programmable RX equalization
- Auto-negotiation
- Link Training
- Excellent random jitter performance
- Robust clock data recovery
- Complete diagnostic suite
  - On-chip PRBS generation and checking
  - RX eye monitor
  - Loop back testing
  - JTAG/IEEE 1500
- MCU per lane

Credo SerDes IP Availability

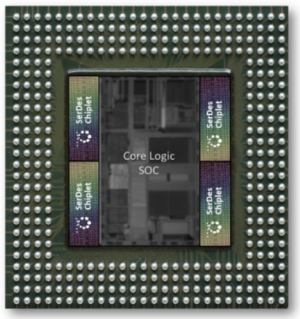
Our IP is designed for a variety of TSMC fabrication processes, data rates and channels losses.

	TSMC 28nm	TSMC 16nm/12nm	TSMC 7/6nm	TSMC 5/4nm
28G NRZ	LR, MR	LR, MR, VSR, XSR	LR, MR, VSR, XSR	LR, MR, VSR, XSR
40G PAM3		LR, MR, VSR		
56G PAM4		LR, MR, VSR, XSR	LR, MR, VSR, XSR	LR, MR, VSR, XSR
112G PAM4		LR, MR, VSR, XSR	XSR	LR, MR, VSR, XSR

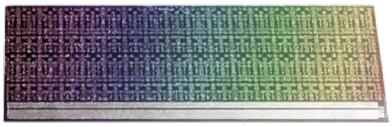
Credo SerDes 3.2Tbps Chiplets

Core and analog logic may not always deploy at the same time in the same process. Maturing high-performance analog typically takes longer in moving to next generation of advanced process geometries. This lagging function may slow the pace of your next generation solutions.

Credo's unique SerDes architecture makes it possible to deliver solutions that are both cost and power effective in mature process nodes. These SerDes solutions are available in chip form for integration with SoCs, overcoming the need for matching core logic and SerDes IP in the same process node.



Now you can fabricate your core logic in advanced processes and combine them in your SoC with Credo SerDes chiplets, designed for high-performance and low-power mature processes. You get the performance needed without delaying time to market.



56G SerDes Chiplet

- 28nm TSMC process
- 2.5D Silicon interposer
- Ideal for 12.8Tbps switch fabric ASIC

112G SerDes Chiplet

- 12nm TSMC process
- MCM/XSR
- Ideal for 25.6Tbps switch fabric ASIC

For more information please visit **www.credosemi.com**
or email **sales@credosemi.com**

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