

**AEC CLOS SPECIFICATION** 

# for In-Rack Ethernet Applications in Distributed, Disaggregated Chassis

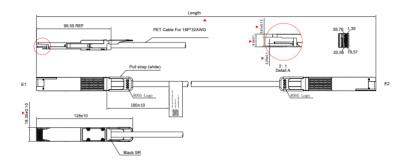
800G QSFP-DD (PAM4) to 800G QSFP-DD (PAM4)



A thin, low power 800G AEC specifically designed for in-rack applications replacing back planes in Distributed, Disaggregated Chassis (DDC) implementations. Plug & Play CLOS AECs consume up to 50% less power than optical and take up to 75% less volume than DACs, enabling interconnect densities of up to 1,000 cables per rack.

With improved reach and signal integrity, these AECs deliver zero soft link flaps to support the lossless backend RDMA network that AI clusters are built on. The ZeroFlap CLOS AEC enables the full host to switch connectivity for leading GPU clusters

Designed for telecom and data center use. It can sustain 8 lanes of 106G-PAM4 signal in each direction, providing bi-directional 800Gbps traffic per cable. The use and replacement of ZeroFlap AEC is simple and straightforward as it adopts standard QSFP-DD type2 form factor and complies to MSA specifications.





### **Features**

The following are the key features of the ZeroFlap CLOS AEC:

- Recognizable, purple PET Mesh jacket
- · 800G to 800G data rate
- · CMIS 5.0 compliant
- · Single 3.3V power supply
- Low power consumption
- Typ. 10W power dissipation each end
- BER < 10<sup>-15</sup> (post FEC)
- Hot pluggable
- · RoHS2 compliant
- · I<sup>2</sup>C management interface
- Operating case temperature range: 0° to +70°C

# Supported Standards and Interfaces

- Common Management Interface Specification (CMIS) v5.0
- · QSFP-DD MSA v5.0

# **Key Features**

Parameter	Value			
Module Form Factor	QSFP-DD type2			
Number of Data Lanes	8 TX and 8 RX per module (PAM4)			
Maximum Aggregate Data Rate	800Gbps			
Nominal Data Rate per Lane	112Gbps (PAM4)			
Electrical Interface and Pin-out	76-pin edge connector			
Pin Description	Per QSFP-DD Hardware Specification			
Management Interface	I <sup>2</sup> C, serial, timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers v 5.0			
Length of Copper AEC	1.0m - 3.0m			
BER (Pre-FEC)*	Typ. <10 <sup>-8</sup>			
BER (Post-FEC)*	<10:15			

<sup>\*</sup> Tested with QPRBS31 pattern

# **Product Selections**

Part Number	Length	Tolerance	CMIS	Weight
CAC81X321M1M-C1-HW	1.0m	±50mm	CMIS 5	175g
CAC815321M1M-C1-HW	1.5m	±50mm	CMIS 5	213g
CAC82X321M1M-C1-HW	2.0m	±50mm	CMIS 5	248g
CAC825321M1M-C1HW	2.5m	±50mm	CMIS 5	288g
CAC827321M1M-C1HW	2.75m	±50mm	CMIS 5	300g
CAC83X321M1M-C1-HW	3.0m	±50mm	CMIS 5	320g

# **About Credo**

Credo's mission is to advance high-speed connectivity solutions that deliver optimized performance, reliability, energy efficiency, and security for the next generation of AI driven applications, cloud computing, and hyperscale networks. Optimized for both optical and electrical applications, our solutions support port speeds up to 1.6Tb. At the core of our technology is our proprietary Serializer/Deserializer (SerDes) IP. Our diverse solutions portfolio includes system-level products such as Active Electrical Cables (AECs), a range of Integrated Circuits, including Retimers, Optical DSPs, SerDes chipsets, and SerDes IP Licensing.

For more information please visit www.credosemi.com or email sales@credosemi.com

