

CLOS AEC SPECIFICATION

PLUG & PLAY ACTIVE ELECTRICAL CABLE

forIn-Rack EthernetApplications in Distributed, Disaggregated Chassis

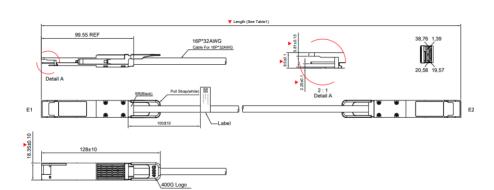
400G CLOS QSFP-DD to 400G QSFP-DD



A thin, low power 400G AEC specifically designed for in rack applications replacing backplanes in Distributed, Disaggregated Chassis (DDC) implementations. Plug & Play LP CLOS AECs consume up to 50% less power than optical and take 75% less volume than DACs, enabling interconnect densities of up to 500 cables per rack.

With improved reach and signal integrity, these AECs deliver zero soft link flaps to support the lossless backend RDMA network that AI clusters are built on. The ZeroFlap AEC enables the full host to switch connectivity for leading GPU clusters

Designed for telecom and data center use. It can sustain 8 lanes of 56G-PAM4 signal in each direction, providing bi-directional 400Gbps traffic per cable. The use and replacement of this AEC is simple and straightforward as it adopts standard QSFP-DD type 2 form factor and complies to MSA specifications.





Features

The following are the key features of the ZeroFlap CLOS AEC:

- Recognizable, purple Mesh Braided jacket
- · 400G to 400G data rate
- · Built-in diagnostic features
- · CMIS compliant
- · Single 3.3V power supply
- Typ.4.5W power dissipation each end
- · BER<10^-15 (postFEC)
- · Hot pluggable
- · RoHS2 compliant
- · I2C management interface
- Operating case temperature range: 0° to +70°C

Supported Standards and Interfaces

- Common Management Interface Specification (CMIS) v4.0
- · QSFP-DD MSA v4.0

Key Features

Parameter	Value			
Module Form Factor	QSFP-DD type 2			
Number of Data Lanes	8 TX and 8 RX per module (PAM4)			
Maximum Aggregate Data Rate	400Gbps			
Nominal Data Rate per Lane	56Gbps (PAM4)			
Electrical Interface and Pin-out	76-pin edge connector			
Pin Description	Per QSFP-DD Hardware Specification			
Management Interface	I ² C, serial, timing per Common Management Interface Specification for 8X/16X Pluggable Transceivers (QSFP-DD)			
Length of Copper AEC	0.5m - 2.5m in 0.5m increments			
BER (Pre-FEC)*	Typ. <10 ⁻⁸ *Tested with QPRBS31 pattern			
BER (Post-FEC)*	<10 ⁻¹⁵ * Tested with QPRBS31 pattern			

Product Selections

Part Number	Length	Tolerance	CMIS	Weight
CAC41X321D1D-D1-HW	1.0m	<u>+</u> 50mm	CMIS 4.0	175g
CAC415321D1D-D1-HW	1.5m	<u>+</u> 50mm	CMIS 4.0	213g
CAC42X321D1D-D1-HW	2.0m	<u>+</u> 50mm	CMIS 4.0	248g
CAC425321D1D-D1-HW	2.5m	<u>+</u> 50mm	CMIS 4.0	288g
CAC43X321D1D-D1-HW	3.0m	<u>+</u> 50mm	CMIS 4.0	315g

About Credo

Credo's mission is to advance high-speed connectivity solutions that deliver optimized performance, reliability, energy efficiency, and security for the next generation of Al driven applications, cloud computing, and hyperscale networks. Optimized for both optical and electrical applications, our solutions support port speeds up to 1.6Tb. At the core of our technology is our proprietary Serializer/Deserializer (SerDes) IP. Our diverse solutions portfolio includes system-level products such as Active Electrical Cables (AECs), a range of Integrated Circuits, including Retimers, Optical DSPs, SerDes chipsets, and SerDes IP Licensing.

For more information please visit www.credosemi.com or email sales@credosemi.com

